

# Claims

[c1] What is claimed is:

1. An audio processing circuit comprising:  
a serial interface having an input for receiving a digital audio signal, and an output for serially outputting bits of the digital audio signal;  
a shift register having a serial input connected to the output of the serial interface for storing bits of the digital audio signal;  
a first-in-first-out (FIFO) buffer having a parallel input connected to a parallel output of the shift register;  
a volume controller connected to the FIFO, the volume controller initiating loading of bits in the shift register into the FIFO according to a volume control signal; and  
a digital-to-analog processor connected to a parallel output of the FIFO.

[c2] 2. The audio processing circuit of claim 1 further comprising an analog amplifier connected to an output of the digital-to-analog processor.

[c3] 3. The audio processing circuit of claim 2 wherein the analog amplifier comprises an operational amplifier having a feedback variable resistance and an input variable

resistance, the feedback variable resistance or the input variable resistance responsive to the volume control signal.

- [c4] 4. The audio processing circuit of claim 3 wherein the volume controller delays or speeds loading of bits in the shift register into the FIFO according to a coarse component of the volume control signal, and the volume controller adjusts the feedback variable resistance or the input variable resistance according to a fine component of the volume control signal.
- [c5] 5. The audio processing circuit of claim 1 wherein the volume controller is further connected to the digital-to-analog processor, and controls the output of the digital-to-analog processor to be a predetermined value when the volume control signal indicates a mute function.
- [c6] 6. An audio processing circuit comprising:  
a serial interface having an input for receiving a digital audio signal, and an output for serially outputting bits of the digital audio signal;  
a shift register having a serial input connected to the output of the serial interface for storing bits of the digital audio signal;  
a first-in-first-out (FIFO) buffer having a parallel input

connected to a parallel output of the shift register;  
a volume controller connected to the FIFO, the volume controller initiating loading of bits in the shift register into the FIFO according to a volume control signal;  
a digital-to-analog processor connected to a parallel output of the FIFO; and  
an analog amplifier connected to an output of the digital-to-analog processor, the analog amplifier comprising an operational amplifier having a feedback variable resistance and an input variable resistance;  
wherein the volume controller delays or speeds loading of bits in the shift register into the FIFO according to a coarse component of the volume control signal, and the volume controller adjusts the feedback variable resistance or the input variable resistance according to a fine component of the volume control signal

7. The audio processing circuit of claim 6 wherein the volume controller is further connected to the digital-to-analog processor, and controls the output of the digital-to-analog processor to be a predetermined value when the volume control signal indicates a mute function.

[c7] 8. A method for adjusting the volume of a digital audio signal comprising:  
serially receiving bits of the digital audio signal;

setting a loading delay according to a volume control signal;  
in parallel, forwarding a segment of the received bits at the expiry of the loading delay; and  
processing the segment of bits into an analog audio signal, wherein the positions of the bits in the segment are directly related to the volume of the analog audio signal.

[c8] 9. The method of claim 8 wherein setting the loading delay comprises lengthening the loading delay to right shift the bits of the segment thereby attenuating the analog audio signal, and shortening the loading delay to left shift the bits of the segment thereby amplifying the analog audio signal, when the serial receiving of bits for the segment is by decreasing order of significance.

[c9] 10. The method of claim 8 wherein setting the loading delay comprises lengthening the loading delay to right shift the bits of the segment thereby amplifying the analog audio signal, and shortening the loading delay to left shift the bits of the segment thereby attenuating the analog audio signal, when the serial receiving of bits for the segment is by increasing order of significance.

[c10] 11. The method of claim 8 further comprising attenuating or amplifying the analog audio signal by an amount less than the unit attenuation or amplification resulting

from a minimum adjustment of the loading delay.

- [c11] 12. The method of claim 8 wherein processing the segment of bits comprises setting each bit of the segment to a predetermined value when the volume control signal indicates a mute function.